CLAIMS:

What is claimed is:

1. An apparatus comprising:

an n-type and a p-type device coupled between first and second supply voltages at a terminal; and

an output node coupled to the terminal, the output node, during operation of the apparatus, to provide an output signal having a switching delay in only one direction that is directly proportional to the leakage current of one of the n-type and p-type devices.

2. The apparatus of claim 1 wherein

the n-type and p-type devices are coupled to function as an inverter.

3. The apparatus of claim 1 wherein

drains of the n-type and p-type devices are coupled to each other at the terminal;

a gate of a first one of the n-type and p-type devices is coupled to receive an input signal, and

a gate of a second one of the n-type and p-type devices is coupled to receive a bias voltage during operation that results in the gate-to-source voltage of the second device being less than the threshold voltage of the second device.

4. The apparatus of claim 3 wherein the gate of the second device is coupled to the source of the second device.

5. The apparatus of claim 1 wherein

a gate of a first one of the n-type and p-type devices is coupled to receive an input signal, and

a gate of a second one of the n-type and p-type devices is coupled to the output node and the source and drain of the second one of the n-type and p-type devices are both coupled to receive one of the first and second supply voltages.

6. The apparatus of claim 1 wherein

a gate of a first one of the n-type and p-type devices is coupled to receive an input signal,

a gate of a second one of the n-type and p-type devices is coupled to receive one of the first and second supply voltages, and

a source and drain of the second device are both coupled to the output node.

7. An apparatus comprising:

a ring oscillator including,

at least one leakage inverter to provide an inverted output signal having a signal transition delay in one direction that is proportional to a leakage current of a device of the first leakage inverter, and

one or more static stages,

the ring oscillator to provide an oscillating output signal.

8. The apparatus of claim 7 wherein

the at least one leakage inverter includes a leaky device having a gate coupled to a receive a bias voltage during operation, the bias voltage being a sub-threshold gate-to-source voltage, and

wherein the leakage current is a drain leakage current.

9. The apparatus of claim 8 wherein

the gate of the leaky device is coupled to receive an enable signal, the leaky device to be turned on in response to the enable signal being deasserted.

10. The apparatus of claim 7 wherein,

the at least one leakage inverter includes a leaky device having a source and drain coupled to receive a supply voltage and a gate coupled to an output node of the leakage inverter, and

wherein the leakage current is a gate leakage current.

11. The apparatus of claim 7 wherein,

the at least one leakage inverter includes a leaky device having a gate coupled to receive a supply voltage and a source and drain coupled to an output node of the leakage inverter.

12. The apparatus of claim 7 wherein,

the ring oscillator includes at least three leakage inverters, and

wherein a frequency of the oscillating output signal varies in proportion to the leakage current of the device.

13. An apparatus comprising:

an enable input to receive an enable signal; and

a leakage ring oscillator to be enabled in response to the enable signal being asserted, the leakage ring oscillator including

at least a first leakage inverter including a leaky device, the leaky device to be substantially fully turned on in response to the enable signal being deasserted; and

an output to provide an oscillating output signal in response to the leakage ring oscillator being enabled, a frequency of the oscillating output signal being dependent upon a leakage current of the first leakage inverter while the leakage ring oscillator is enabled.

14. The apparatus of claim 13 wherein the leakage ring oscillator includes at least three leakage inverters, each of the three leakage inverters including a leaky device to be substantially fully turned on and another device to be substantially fully turned off in response to the enable signal being deasserted.

15. The apparatus of claim 14 wherein at least one of the three leakage inverters includes a device coupled to receive a sub-threshold gate-to-source voltage in response to the enable signal being asserted.

16. The apparatus of claim 14 wherein at least one of the three leakage inverters includes a device having a source and drain coupled to receive a same supply voltage and a gate coupled to an output of the leakage inverter.

17. The apparatus of claim 14 wherein at least one of the three leakage inverters includes a device having a gate coupled to receive a supply voltage and a source and drain both coupled to an output of the leakage inverter.

18. The apparatus of claim 14 wherein at least one of the three leakage inverters is coupled such that the leakage current is a drain leakage current.

19. The apparatus of claim 14 wherein at least one of the three leakage inverters is coupled such that the leakage current is a gate leakage current.

20. An integrated circuit comprising:

a plurality of leakage ring oscillators, each of the leakage ring oscillators including at least a first leakage inverter to provide an inverted output signal

having a transition delay in one direction that is proportional to a leakage current of a device of the leakage inverter, each of the plurality of leakage ring oscillators to provide an oscillating output signal, a frequency of the respective oscillating output signal to indicate at least one of a local temperature and leakage current; and

an externally-accessible output circuit coupled to receive the oscillating output signal.

21. The integrated circuit of claim 20 wherein the externally-accessible output circuit is a test access port.

22. The integrated circuit of claim 20 wherein the externally-accessible output circuit includes a control register.

23. The integrated circuit of claim 20 wherein

at least one of the leakage ring oscillators includes at least three leakage inverters.

24. The integrated circuit of claim 23 wherein the at least three leakage inverters indicate local gate leakage.

25. The integrated circuit of claim 23 wherein the at least three leakage inverters indicate local channel leakage.

26. A method comprising:

detecting a frequency of a leakage ring oscillator on an integrated circuit, the leakage ring oscillator including at least a first leakage inverter to provide an inverted output signal having a transition delay in one direction that is proportional to a leakage current of a device of the leakage inverter over a first temperature range; and

determining one of a local temperature or relative leakage current in response to the detected frequency.

27. The method of claim 26 wherein determining comprises

accessing data indicating leakage ring oscillator frequency versus at least one of temperature and leakage current.

28. The method of claim 26 further comprising:

characterizing each of the leakage ring oscillators at different temperatures; and

developing a look-up table indicating frequency of the oscillating output signal versus temperature.